REMARKS

Applicants have studied the Office Action dated September 26, 2003 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-21 and 30-39 are pending. Claims 1, 9, 14-21, and 35 have been amended, and new claims 36-39 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

As an initial matter, Applicants note that an initialed copy of the PTO-1449 form that was submitted along with the present application has not been attached to an Office Action to indicate that all of the references listed in the PTO-1449 form were considered by the Examiner. This PTO-1449 form lists the references that were cited by both the Examiner and Applicants during prosecution of the parent application. Because this list of references was submitted at the time of filing of the present application, under 37 C.F.R. § 1.97(b) the Examiner must consider the listed references. Accordingly, Applicants request that the Examiner consider the references listed in the PTO-1449 submitted along with the present application and attach to the next correspondence an initialed copy of the PTO-1449 form to indicate that all of the listed references have been considered. For the convenience of the Examiner, enclosed is a copy of the PTO-1449 form that was submitted along with the present application.

Turning to the patentability of the application, claims 1-21 and 30-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. (U.S. Patent No. 6,255,702). This rejection is respectfully traversed.

The present invention is directed to processes for forming a low resistivity titanium silicide layer at the surface of a silicon semiconductor substrate. One embodiment of the present invention provides a method for forming a low resistivity titanium silicide layer on a surface of at least one previously doped region of a silicon semiconductor substrate. According to the

method, a titanium layer is deposited on the surface of the doped region of the silicon semiconductor substrate (which was previously doped to form an n-type or p-type source or drain region), and a rapid thermal annealing of the silicon semiconductor substrate coated with the titanium layer is performed in order to form titanium silicide.

Before the step of performing the rapid thermal annealing, an effective amount of a metallic element is introduced at least at the interface between the titanium layer and the doped region of the silicon semiconductor substrate, with the metallic element being chosen from the group consisting of indium, gallium, tin, and lead. The rapid thermal annealing step anneals the titanium layer with the introduced metallic element so that the introduced metallic element promotes titanium silicide transformation from C49 phase to C54 phase during the rapid thermal annealing. Because the introduced metallic element is subjected to annealing concurrently with the deposited titanium layer, titanium silicide transformation from the C49 phase to the C54 phase is promoted during the annealing. Thus, a low resistivity titanium silicide layer is formed on the surface of the previously doped region of the silicon semiconductor substrate.

The Iwata reference discloses a process for forming a semiconductor device in which a silicon nitride film is used in place of a silicon oxide film. However, Iwata does not disclose a method in which a titanium layer is deposited on the surface of an n-type or p-type previously doped region of a silicon semiconductor substrate, a rapid thermal annealing of the titanium-coated substrate is performed in order to form titanium silicide, and before the annealing an effective amount of indium, gallium, tin, or lead is introduced at least at the interface between the titanium layer and the doped region of the silicon semiconductor substrate, with the rapid thermal annealing acting to anneal the titanium layer with the introduced metallic element so that the introduced metallic element promotes titanium silicide transformation from C49 phase to C54 phase during the annealing, as is recited in amended claim 1.

Similarly, Iwata does not disclose a method in which at least one region of a silicon semiconductor substrate is doped with a first metallic element to form an n-type or p-type source or drain region, and after the doping a low resistivity titanium silicide layer is formed on the surface of the at least one doped region, with the titanium silicide layer being forming by a

process that includes depositing a titanium layer on the surface of the at least one doped region, performing a rapid thermal annealing of the titanium-coated silicon semiconductor substrate in order to form titanium silicide, and before the annealing introducing an effective amount of a second metallic element chosen from the group consisting of indium, gallium, tin, and lead at least at the interface between the titanium layer and the at least one doped region, with the rapid thermal annealing acting to anneal the titanium layer with the second metallic element so that the second metallic element promotes titanium silicide transformation from C49 phase to C54 phase during the annealing, as is recited in amended claim 15.

Likewise, Iwata does not disclose a method in which a titanium layer is deposited on the surface of a silicon semiconductor substrate, an effective amount of indium, gallium, tin, or lead is introduced at least at the interface between the titanium layer and the silicon semiconductor substrate, and after the depositing and introducing there is performed a single rapid thermal annealing of the silicon semiconductor substrate coated with the deposited titanium layer so as to form C54 phase titanium silicide from the deposited titanium layer, with the annealing acting to anneal the titanium layer with the introduced metallic element so that the introduced metallic element promotes titanium silicide transformation from C49 phase to C54 phase during the single rapid thermal annealing, as is recited in amended claim 35.

First, Applicants would like to point out two typographical errors in Iwata that are quoted by the Examiner to make sure there is no misunderstanding as to what is taught. At column 29, lines 42-46, Iwata states that "impurity ions, e.g., indium, 409 as an acceptor for the silicon semiconductor substrate, was implanted into the n-channel region, or the n-well at a dose of approximately $1\text{-}5\times10^{14}/cm^2$ with an energy of 40-80 keV (See FIG. 14 (d))" (emphasis added). However, the Iwata reference does not actually contain a "Figure 14(d)" and reference numeral "409" is used to refer to arsenic ions in the previous paragraph describing Figure 14(c). The quoted portion of the description of Iwata actually refers to Figure 15(d) and the indium ions are actually labeled with reference numeral 411. Thus, Iwata teaches implanting arsenic ions 409 into the left side of the substrate in Figure 14(c), and implanting indium ions 411 into the right side of the substrate in Figure 15(d).

Iwata is directed to a semiconductor device fabrication process in which source or drain regions are doped with donors or acceptors through a silicon nitride film rather than a silicon oxide film. See Iwata at 4:9-14. Figures 14(a) through 17(k) of Iwata disclose two separate processes for forming a silicide layer. The right side of theses figures discloses a first fabrication process in which:

a silicon nitride film 407 is deposited (Figure 14(b)),

indium or boron ions 411 are implanted as acceptor for the silicon semiconductor substrate (Figure 15(d)),

side wall spacers 412 are formed (Figure 15(e)),

a thermal anneal is performed at 900°C (Figure 16(g)),

the silicon nitride film is removed,

a titanium film 416 is deposited (Figure 16(h)),

silicon is ion implanted to mix silicon and titanium in the vicinity of the interface to smoothen the initial stage of silicidation reaction,

a first thermal anneal is performed at 675 °C to form a titanium silicide film 418 of the C-49 type in the silicon (Figure 16(i)),

boron 420 is implanted as impurity ions as acceptor for the silicon semiconductor substrate (Figure 17(j)),

the titanium nitride film 417 is removed, and

a second thermal anneal is performed at 1000°C to transform the titanium silicide film 418 into the C-54 type (Figure 17(k)).

Thus, in this first process of Iwata, the substrate is p-type doped with indium, the doped region is annealed, a titanium film is deposited, the substrate is ion implanted with silicon ions to mix silicon and titanium in the vicinity of the interface to smoothen the initial stage of silicidation reaction, a first thermal anneal is performed for silicidation of the titanium layer, boron is implanted as impurity ions, and then a second thermal anneal is performed for silicidation of the titanium layer.

A second fabrication process is disclosed in the left side of Figures 14(a) through 17(k) of Iwata. In the second fabrication process:

a silicon nitride film 407 is deposited (Figure 14(b)),

arsenic ions 409 are implanted to form shallow junctions in the vicinity of the channel region (Figure 14(c)).

side wall spacers 412 are formed (Figure 15(e)),

arsenic ions 414 are implanted as a donor for the silicon semiconductor substrate (Figure 15(f)),

a thermal anneal is performed at 900°C (Figure 16(g)),

the silicon nitride film is removed,

a titanium film 416 is deposited (Figure 16(h)),

silicon is ion implanted to mix silicon and titanium in the vicinity of the interface to smoothen the initial stage of silicidation reaction,

a first thermal anneal is performed at 675 °C to form a titanium suicide film 418 of the C-49 type in the silicon (Figure 16(i)),

the titanium nitride film 417 is removed, and

a second thermal anneal is performed at 1000°C to transform the titanium silicide film 418 into the C-54 type (Figure 17(k)).

Thus, in this second method of Iwata, a substrate is n-type doped with arsenic, the doped region is annealed, a titanium film is deposited, the substrate is ion implanted with silicon ions to mix silicon and titanium in the vicinity of the interface to smoothen the initial stage of silicidation reaction, and first and second thermal anneals are performed for silicidation of the titanium layer.

In contrast, in preferred embodiments of the present invention, a titanium layer is deposited on a region of the substrate that has been previously doped to form an n-type or p-type source or drain region, Thus, the region is electrically doped before the titanium is deposited (such as by conventionally implanting boron, indium, or arsenic, and then annealing to obtain the electrical doping effect). In preferred embodiments of the present invention, an effective amount of indium, gallium, tin or lead is introduced at the interface between the titanium layer and the

previously doped region, and after the metallic element is introduced a rapid thermal anneal is performed in order to form titanium silicide.

In this rapid thermal anneal, the introduced metallic element (i.e., indium, gallium, tin or lead) is annealed with the deposited titanium layer. In other words, the introduced metallic element is subjected to annealing concurrently with the deposited titanium layer; it is not annealed before the titanium layer is deposited. This concurrent annealing operation provides advantages due to the unconventional metallurgical properties of the introduced metallic element, with respect to alloying with titanium and silicon. In particular, indium, gallium, tin and lead have proven to be metallurgically favorable for promoting titanium silicide transformation from the C49 phase to the C54 phase during the concurrent thermal annealing operation.

Iwata does not teach or suggest a fabrication process for forming a low resistivity titanium silicide layer on a previously doped region that includes depositing a titanium layer on the previously doped region, introducing an effective amount of indium, gallium, tin or lead at the interface between the titanium layer and the previously doped region, and performing thermal annealing so as to concurrently anneal the deposited titanium layer and the introduced metallic element. Iwata discloses fabrication processes in which a region is electrically doped by implanting ions and then performing thermal annealing, a titanium layer is deposited, ions of silicon are implanted, and then thermal annealing is performed to form a titanium silicide layer. Further, in the fabrication processes of Iwata, two thermal annealing operations must be performed in order to obtain C54 phase titanium silicide from the deposited titanium layer.

Applicants believe that the differences between Iwata and the present invention are clear in amended claims 1, 15, and 35, which set forth methods according to various embodiments of the present invention. Therefore, claims 1, 15, and 35 distinguish over the Iwata reference, and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

As discussed above, claims 1 and 15 distinguish over the Iwata reference, and thus, claims 2-14 and 30-32, and claims 16-21, 33, and 34 (which depends from claim 1 and 15,

respectively) also distinguish over the Iwata reference. Additionally, Applicants submit that limitations added by the dependent claims are not taught or suggested by the Iwata reference.

For example, claims 7 and 18 recite that the metallic element is deposited on the surface of the doped region of the silicon semiconductor substrate. Iwata does not teach or suggest depositing indium, gallium, tin, or lead at the surface of a previously doped region of a substrate.

Likewise, claims 9 and 14 recite that the metallic element is introduced before the titanium layer is deposited, and the introduced metallic element is not thermally annealed before the titanium layer is deposited.[1] Iwata does not teach or suggest a fabrication process in which indium, gallium, tin, or lead is introduced before, and not thermally annealed before, a titanium layer is deposited.

Further, the Examiner did not offer any explanation as to how Iwata reads on the limitations recited in dependent claims 30-34. Accordingly, the Examiner failed to make out a prima facie case of obviousness with respect to claims 30-34. Additionally, claims 30, 31, 33, and 34 add the limitation that the doped region is an n-type region or the doped region is doped with arsenic. Iwata does not teach or suggest introducing indium, gallium, tin, or lead into an n-type region or a region doped with arsenic. Such a feature is contrary to the conventional teaching of using such elements as acceptors in p-type regions, and not adding them to an n-type region. However, this feature produces very advantageous, unexpected results. For example, Figure 2 shows the advantageous results obtained when indium was implanted as a silicidation promoter in an arsenic-doped n-type region. Likewise, claim 32 recites that the metallic element is gallium, tin, or lead. Iwata does not teach or suggest introducing gallium, tin, or lead into a doped region of the silicon semiconductor substrate.

Therefore, it is respectfully submitted that the rejection of claims 1-21 and 30-34 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 36-39 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 36-39 are allowable for at least the reasons set

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[1] New claim 38 contains similar recitations.

forth above with respect to claims 1-21 and 30-35. Furthermore, Applicants submit that limitations added by the new claims are not taught or suggested by the Iwata reference. For example, new claims 36 and 37 recite that the metallic element is introduced after the titanium layer is deposited, and the deposited titanium layer is not thermally annealed before the metallic element is introduced. Iwata does not teach or suggest a fabrication process in which a titanium layer is deposited before, and not thermally annealed before, indium, gallium, tin, or lead is introduced.

Therefore, it is respectfully submitted that claims 36-39 are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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